Intel in HPC and CERN Openlab

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2007+ Intel in HPC

- High End (up to PetaScale):
 - Dedicated technical expertise for high end solutions
 - -Collaborate with key institutions & industry consortia
 - Drive performance leadership & broader technology pipeline
- Volume: HPC fastest server growth segments
 - -Enable customers & channel with differentiated Solutions;
 - >HW: processors, Boards, Systems.
 - >SW: Libraries, compiler, tools, app optimization,



Intel & CERN Openlab

- Public activities
 - 3rd Intel EMEA HPC end user Roundtable May 06
 - Hosted Intel Quad core launch at CERN (with press) (Nov 06)
 - Joint talk at SC'06 conference in Tampa, US, November 2006
- Detailed work
 - SW, Virtualization
 - > Virtualization in batch subsystems
 - > Testing Xen paravirtualization and VT extensions new machines
 - Montecito / VT-i
 - Dempsey / VT-x
 - > Compiler advanced testing / optimization
 - Future Products and technology: CERN application analysis and prediction
 - Joint 2 day Multi-Threading training course planned for May 31st June 1st, 2007
- High level
 - Craig Barrett visit February 2007
 - Justin Rattner Technology key-note talk at CERN, September 2006
 - Power efficient computing Pat Gelsinger visit
 - Visit of Key CERN members at Intel (Apr 07)
 - > Update re. new technologies
- CERN Production Systems
 - 700 node System number 8.3 Tflops on top500 (Nov List)
 - Quadcore testing

Thanks for the good and productive collaboration



Technology direction to mention ... just a few things

Performance

- Manufacturing Process: 45nm
- Many core;
- Highly parallel, IA-based programmable architecture
- -PCI Gen 2
- Intel® QuickAssist Technology a comprehensive initiative to optimize the use of accelerators in servers.

Operating Environment

- Virtualization
 - > HW assist, Ecosystem
- Security
- Manageability



To comejust to name a few.

- Continued testing new HW and SW technology>E.g. Penryn testing
- -GEANT4 ACC application characterization
- Common performance counter interface under Linux
- FP7
- Potential additional multi-threading training class

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